Rafael Peria de Sene
Technical Program Manager
The Linux Foundation | RISC-V International
rsene@linuxfoundation.org or rafael@riscv.org
@rpsene
May, 2024

About Me

Computer Science + MBAs (Project Management, Data Protection, Production Engineering)

IBM + RedHat
The Linux Foundation + RISC-V
Love Cycling

RISC-V®

What is RISC-V?

The RISC-V Instruction Set Manual
Volume I: Unprivileged ISA
Document Version 20191213

Editors: Andrew Waterman[1], Krste Asanović[1,2]
[1]SiFive Inc.,
[2]CS Division, EECS Department, University of California, Berkeley
andrew@sifive.com, krste@berkeley.edu
December 13, 2019

RISC-V®

What is RISC-V?

The RISC-V Instruction Set Manual
Volume I: Unprivileged ISA
Document Version 20191213

Editors: Andrew Waterman[1], Krste Asanović[1,2]
[1]SiFive Inc.,
[2]CS Division, EECS Department, University of California, Berkeley
andrew@sifive.com, krste@berkeley.edu
December 13, 2019

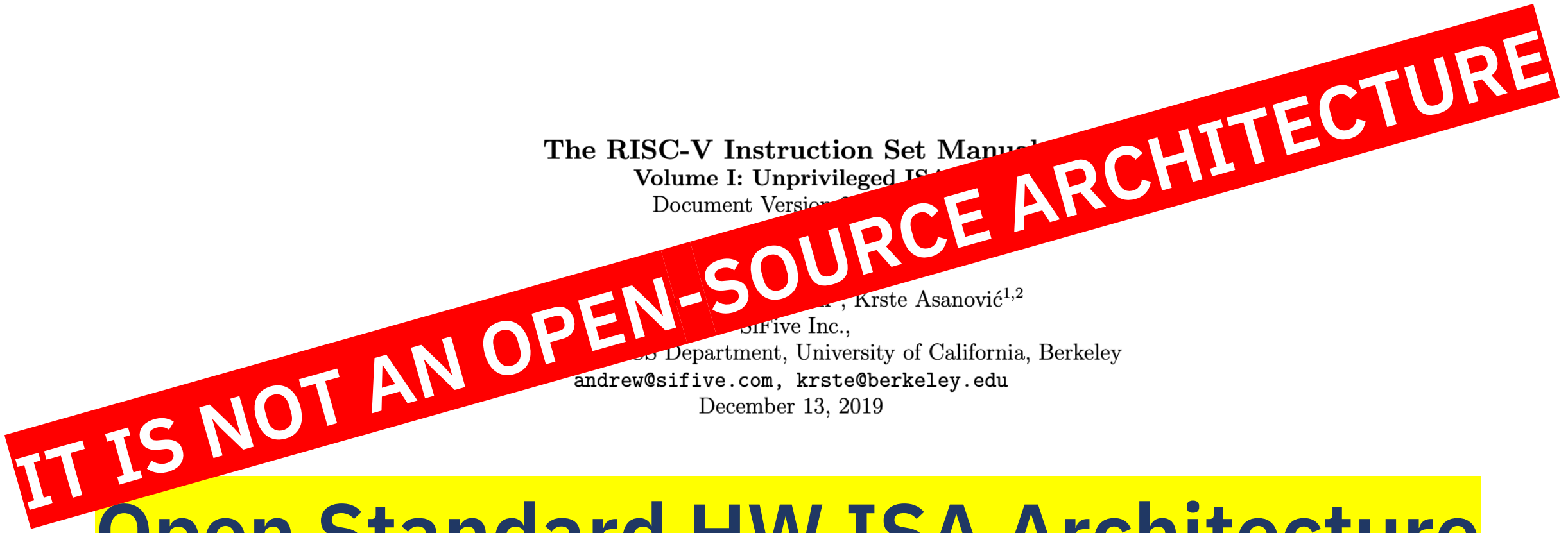
Open Standard HW ISA Architecture

RISC-V®

What is RISC-V?

ISO, the International Organization for Standardization, defines standards as "a document that provides requirements, specifications, guidelines or characteristics that can be used ***consistently*** to ensure that materials, products, processes and services are fit for their purpose."

What is RISC-V?


The RISC-V Instruction Set Manu
Volume I: Unprivileged IS
Document Versio
, Krste Asanović[1,2]
SiFive Inc.,
Department, University of California, Berkeley
andrew@sifive.com, krste@berkeley.edu
December 13, 2019

IT IS NOT AN OPEN-SOURCE ARCHITECTURE

Open Standard HW ISA Architecture

RISC-V®

Open standards are accepted practice

Field	Proprietary Predecessor	Open Standard	Open Implementation	Commercial Implementation on Open Standard
Networking	Now obsolete	Ethernet, TCP/IP	Many	Cisco, Juniper
OS	Windows	Posix	Linux, FreeBSD	Red Hat, Canonical, Suse, AIX, Zephyr
Compilers	Intel icc, ARMcc, Xcode	C	gcc, LLVM	Greenhills, IAR
Databases	Oracle 12C, DB2	SQL	MySQL, PostgresSQL	Oracle, SQLServer, DB2
Graphics	DirectX	OpenGL	Mesa3D	NVIDIA, AMD, Intel
ISA	x86, ARM, IBM360	RISC-V	LowRISC, other community led	Numerous RISC-V implementations

RISC-V®

Once you move to high-quality open standard, you don't move back to proprietary single-source standard.

On May 18th RISC-V is turning 14! To celebrate we are **giving away 14 bundles of the RISC-V Fundamentals Course and RISC-V Foundational Associate Certification (RVFA)**. We would love to support your RISC-V Learning journey through this opportunity so **apply here** by May 22nd at 11:59 PM Pacific. Individuals will be entered into a pool from which winners will be selected randomly.

Enter for a Chance to Win!

https://bit.ly/riscv-win

RISC-V®

Who is RISC-V?

RISC-V International is a global nonprofit association based in **Switzerland**. Founded in 2015, RISC-V brings together **4K+ members** in more than 70 countries across industries and technical disciplines.

- **Drive progression of ratified specs, compliance suite, and other technical deliverables;**
- **Grow the overall ecosystem/membership, promoting diversity while preventing fragmentation;**
- **Deepen community engagement and visibility;**

ISA Specification	Golden Model	Compatibility

Why is RISC-V so popular?

- Movement **is not** happening because some benchmark ran 10% faster, or some implementation was 30% lower power (though this might be true).

- Movement is happening because **new business model changes everything**:
  - **Pick ISA first**, then pick vendor or build own core;
  - **Add your own extension** without getting permission;
  - Commercial, academic, and open-source ecosystems can **coalesce around a single open standard**.

Specifications in Progress Today: 53 | tech.riscv.org

RISC-V®

Standardization and modularity for best in class implementations

Open standard IP specifications for modular designs based on decades of investment and expertise

Open software
Applications, Linux support, libraries/platforms

General and differentiated software
Expertise, applications, services

Academic + Research implementations

General and differentiated implementations
IP, SoC, FPGA, enhanced functions

Open design tools + software

Leading industry design tools + software
Compilers, Simulators, Tools,

Open IP and cores
Provided via ecosystem

Commercial IP and cores
for differentiated performance and capabilities

Modular IP specifications + Architecture compatibility tests
Profiles, extensions incl Vector, Security, Memory, Trace + Debug

RISC-V Instruction Set Architecture (ISA) Open Standard

Commercial innovation and differentiation to solve full spectrum of compute challenges

RISC-V®

Vertical Semiconductor Era

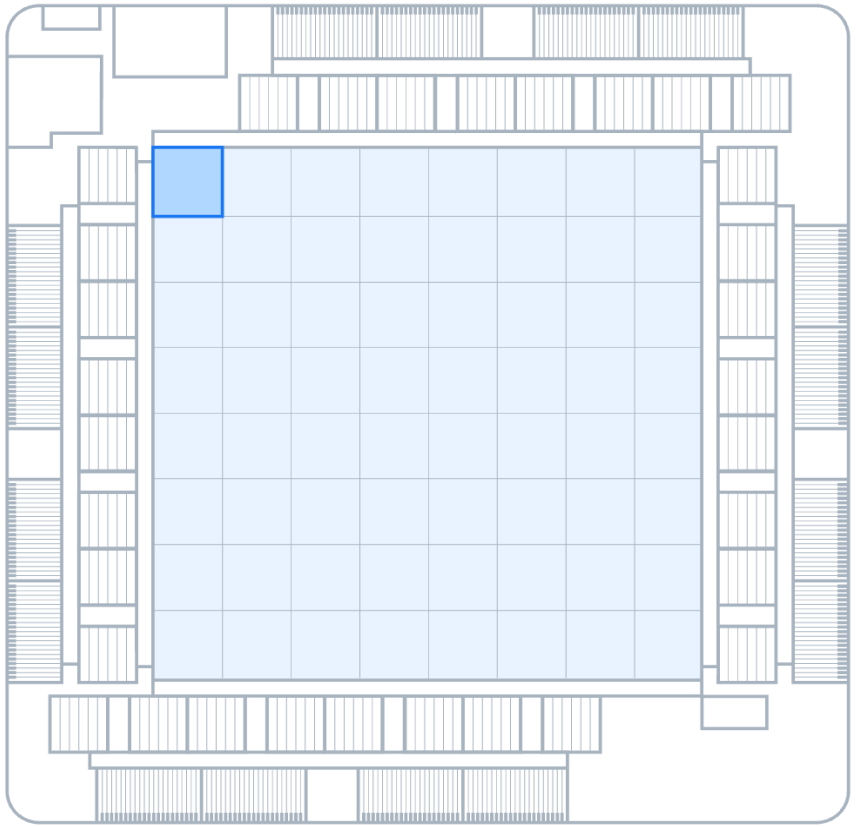
Instead of using chip company's standard parts, product companies build its own differentiated silicon systems.

End-system sales justifies chip design costs, not chip sales.

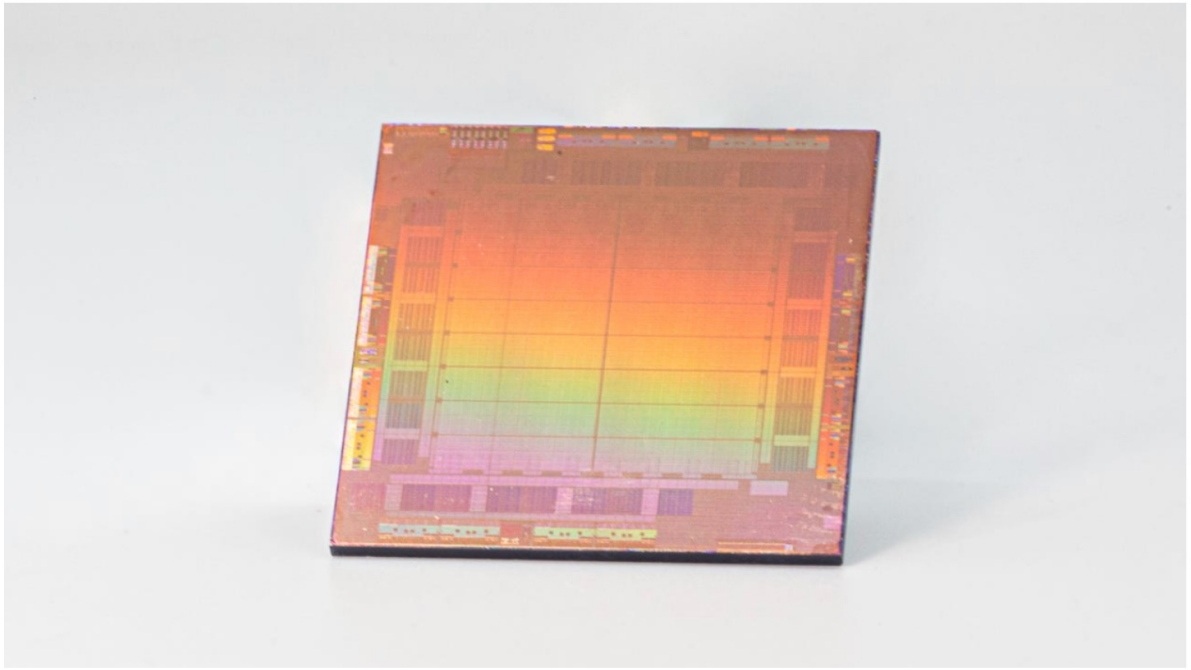
RISC-V®

Each PE is equipped with two processor cores (one of them equipped with the vector extension) and a number of fixed-function units that are optimized for performing critical operations, such as matrix multiplication, accumulation, data movement, and nonlinear function calculation. The processor cores are based on the RISC-V open instruction set architecture (ISA) and are heavily customized to perform necessary compute and control tasks.

Each PE also has 128 KB of local SRAM memory for quickly storing and operating on data. The architecture maximizes parallelism and data reuse, which are foundational for running workloads efficiently.



End-system justifies chip design costs, not chip sales.



Tech News: Meta's 2nd-Gen AI Chip with RISC-V Core, Launching 2026

End-system justifies chip design costs, not chip sales.

Google to use RISC-V for its custom AI silicon — TPU to get open source compute core: Report

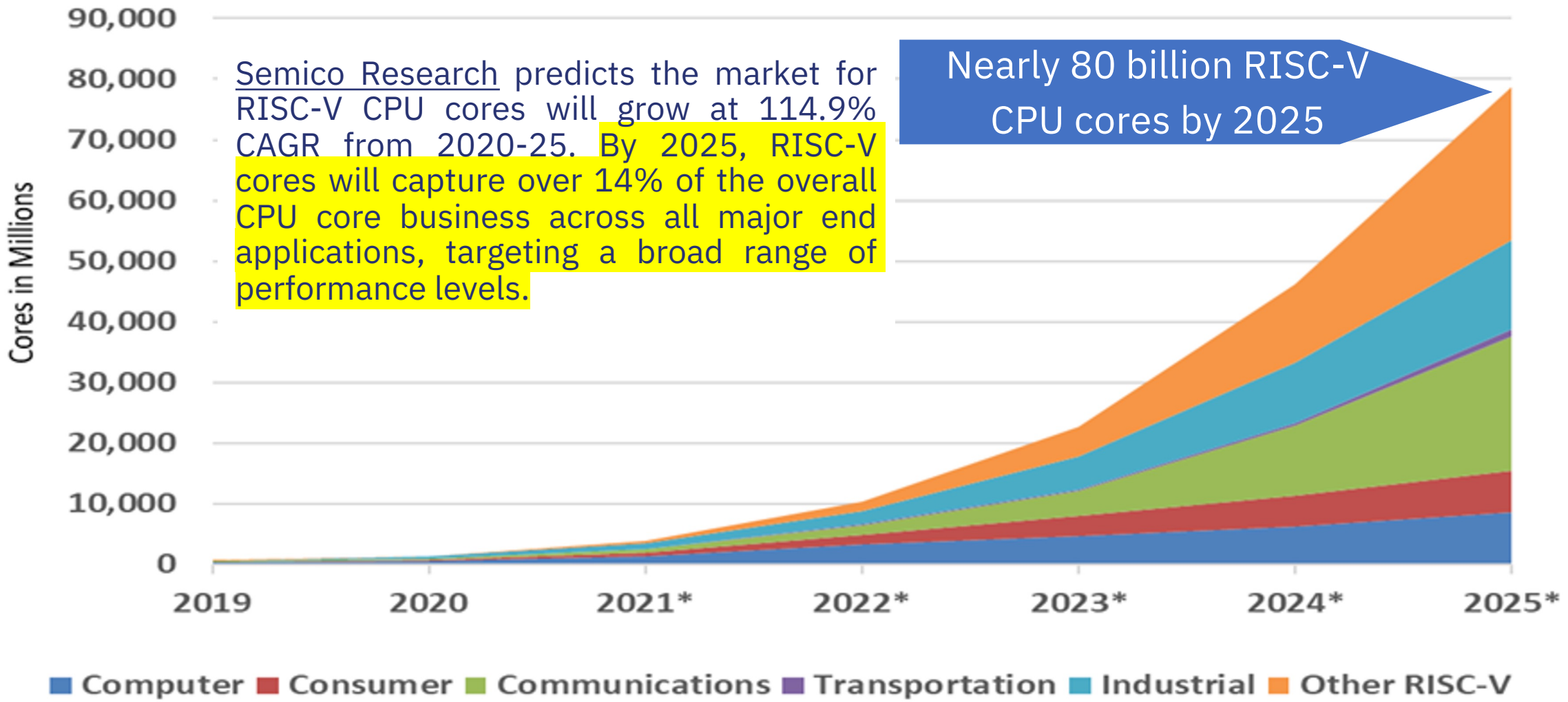
News By Anton Shilov published March 15, 2024

SiFive expected to earn from $240 million to $280 million in 2024.

End-system justifies chip design costs, not chip sales.

Rapid RISC-V growth

Semico Research predicts the market for RISC-V CPU cores will grow at 114.9% CAGR from 2020-25. By 2025, RISC-V cores will capture over 14% of the overall CPU core business across all major end applications, targeting a broad range of performance levels.



Rapid RISC-V growth

PR Newswire Send a Release

RISC-V adoption will be accelerated by AI, according to new Omdia research

OMDIA
Brought to you by Informa Tech

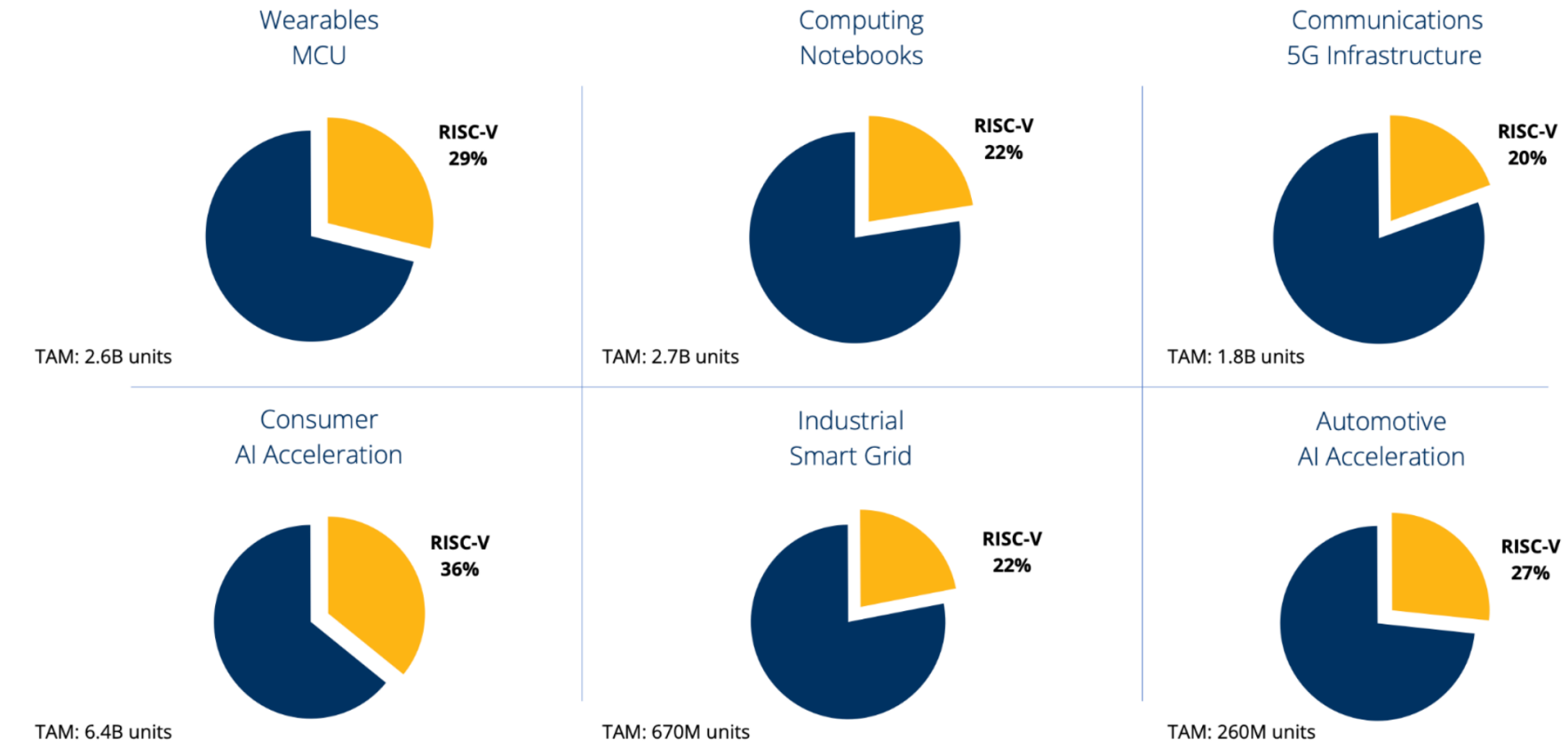
NEWS PROVIDED BY
Omdia →
May 16, 2024, 10:27 ET

Between 2024 and 2030, Omdia forecasts RISC-V-based processor shipments to increase by nearly 50% per year, culminating in 17 billion processors shipped in 2030. 46% of those processors are expected to be found in industrial applications, although the biggest growth over the forecast period will come in the automotive segment.

LONDON, May 16, 2024 /PRNewswire/ -- RISC-V processors will account for almost a quarter of the **global market** by 2030, according to **new research by Omdia**. The open-standard instruction set architecture (ISA) is predicted to experience the strongest growth in the automotive sector, although the industrial space will remain the largest application for the technology. Additionally, the rise of Artificial Intelligence (AI) is instrumental in the continued rise of RISC-V.

RISC-V®

Rapid RISC-V Growth
Market Share Projection in 2030



Source: The SHD Group, November, 2023

Based on projected SoC volumes

Ready to Tackle Real-World Applications

RISC-V®

Automotive

mobileye™

ADAS chips capable of 176 trillion ops per second with 12 RISC-V CPU cores

imperas

NSITEXE selects ImperasDV for advanced RISC-V processor hardware design verification

Imagination

SoC.one and Imagination partner to enable adoption of RISC-V for automotive applications

IAR SYSTEMS

RISC-V Embedded Workbench for SiFive infotainment, connectivity, and ADAS products

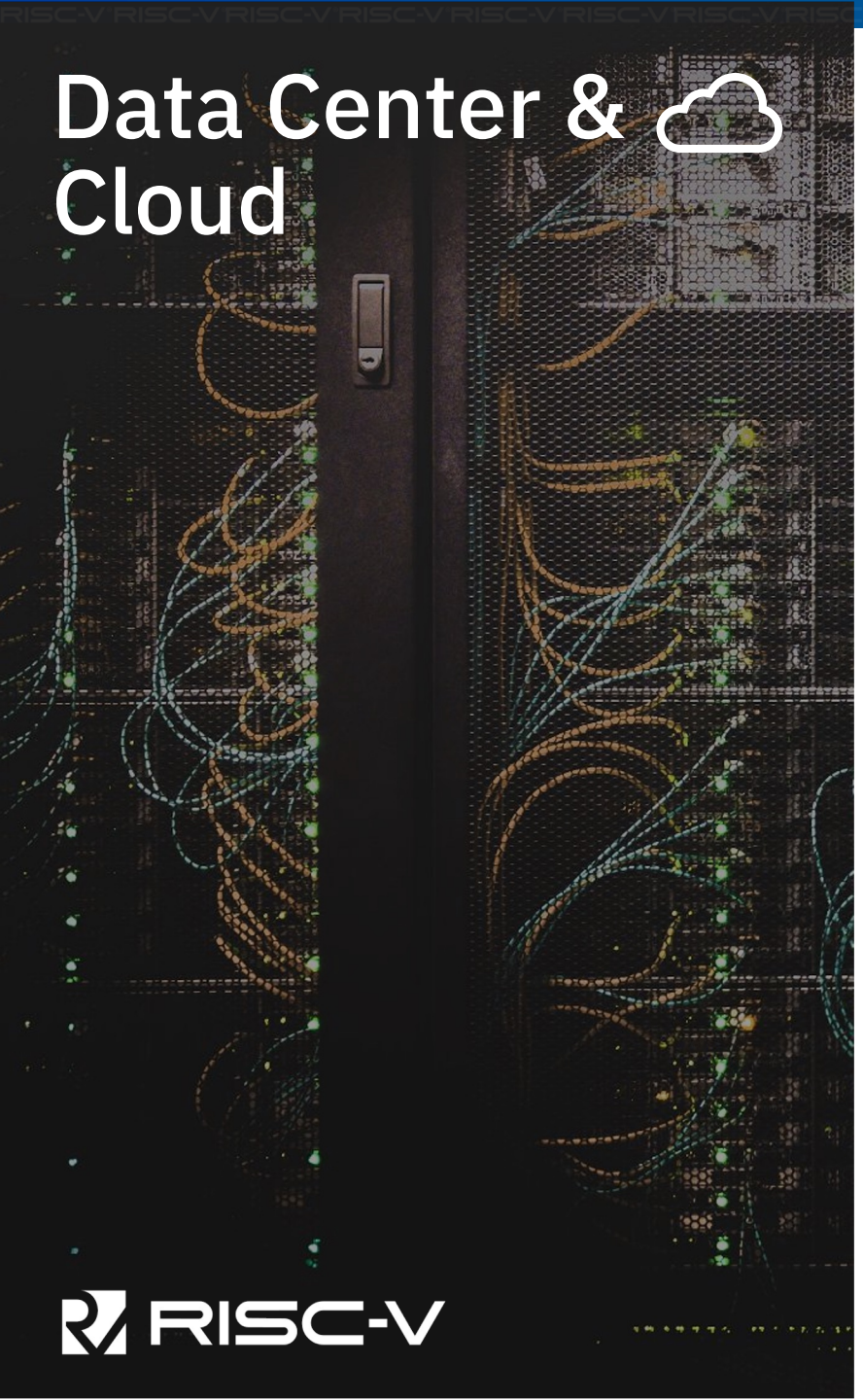
SiFive

Automotive portfolio announced targeting cockpit electrification, ADAS, safety, and others applications

MIPS ELEVATING RISC-V

eVocore CPUs for high-performance, real-time compute in datacenter and automotive

RISC-V



Data Center & Cloud

esperanto.ai

1,000-Core RISC-V AI accelerator designed for data centers

intel

Transforms the way SOC architects and system software developers define new products

Imagination

RISC-V Catapult cores address a range of markets including data center and high performance computing

VENTANA MICRO

Performance chiplet approach to data center high performance SoC design

Alibaba

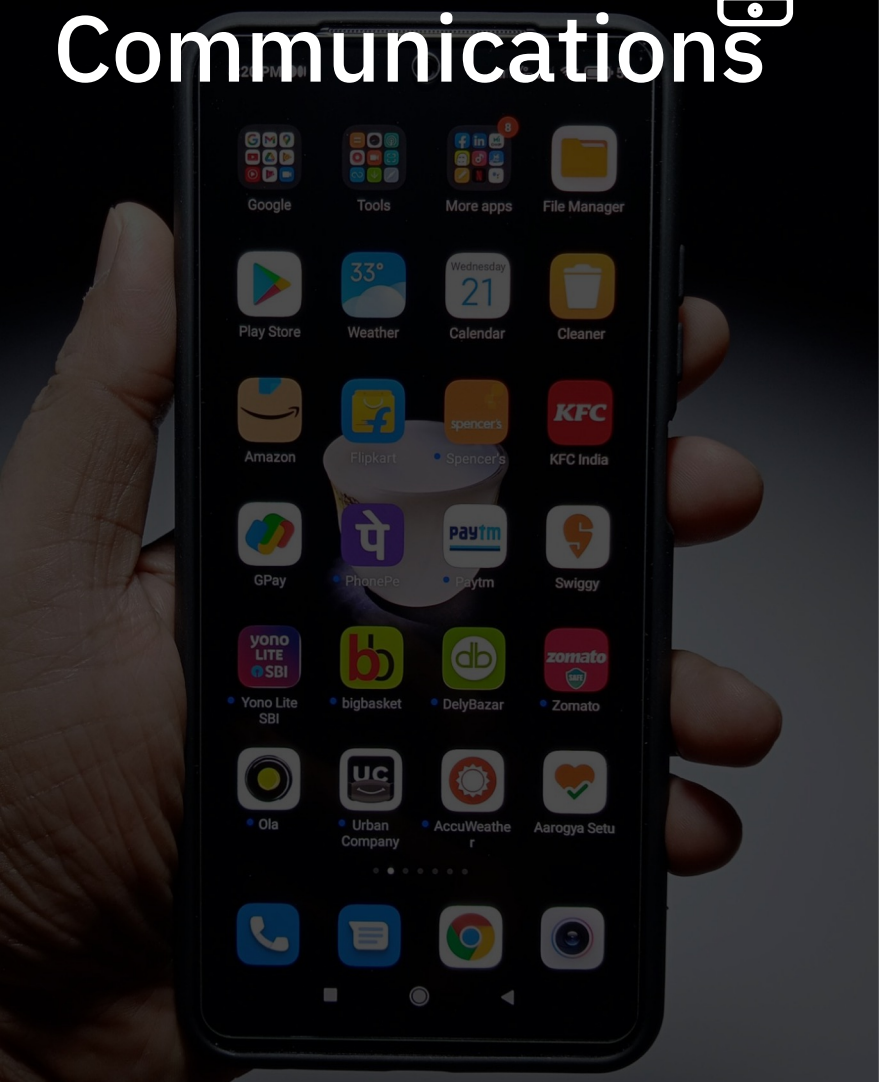
RISC-V Xuantie processors with 4 open cloud and edge processors

ANDES TECHNOLOGY

AndesCore AX65 targets high performance applications including data center

RISC-V

Telecom & Communications



ESPRESSIF

First Dual-Band Wi-Fi 6 and BLE RISC-V chip

RISC-V chip runs Android 10, with RV64 phone coming next

Alibaba

Supporting Android 12 on their 64-bit RISC-V core emulated in QEM

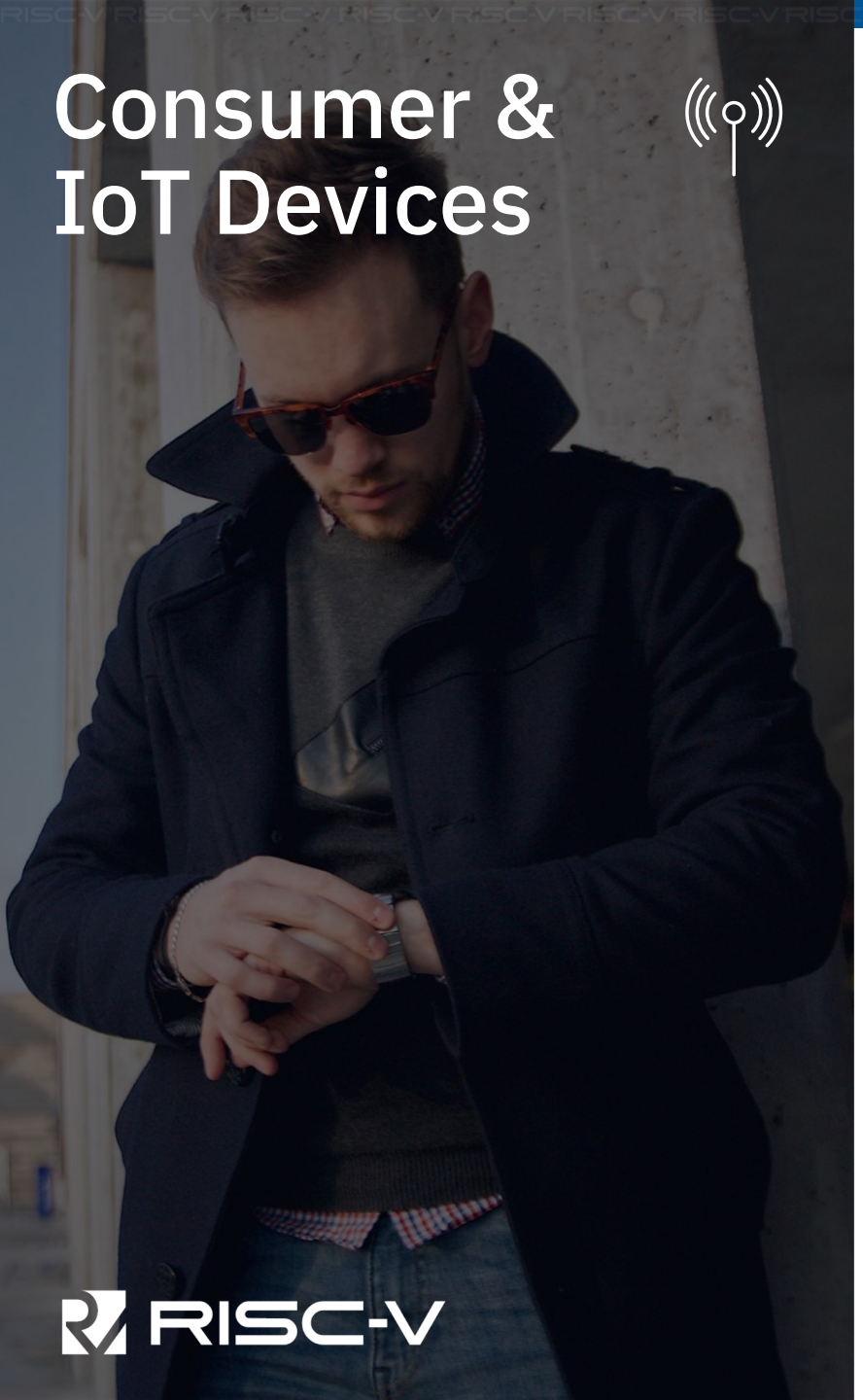
Pixel 6 Titan M2 RISC-V processor, with extra speed and memory, more resilient to advanced attacks

ANDES TECHNOLOGY

EdgeQ using AndesCore™ RISC-V license to deliver industry's first fully open and programmable 5G platform with integrated AI

RISC-V

Consumer & IoT Devices



Android Open Source Project (AOSP) ported to RISC-V

ESP8684 RISC-V WiFi & BLE MCU in 4x4mm package

DeepComputing ROMA is first RISC-V Laptop

Dolphin Design has teams up with Sonical for platform for next generation hearables

P670 and P470 for wearables, smart home, VR, Industrial IoT

PolarFire SoC portfolio of multi-core RISC-V SoC FPGA addresses low power embedded and IoT applications

Sig-Android / Messages

Single | Topic Properties | Mute

Re: RISC-V support in Androing GKI being dropped ??

enh

On Tue, Apr 30, 2024 at 10:52 AM enh <enh@...> wrote:

> what is true is:
>
> * nothing has changed with our work on Android/riscv64 support in AOSP
>
> * we've stopped producing ACK/GKI builds for now
>
> * until there is an official GKI kernel, we're working on
> transitioning to a kernel that we -- the folks working on
> Android/riscv64 -- maintain...

specifically see here:
https://android-review.googlesource.com/c/kernel/common/+/3070126

> * ...but unfortunately the GKI changes went out before our changes are ready
>
> note that the "non-GKI" kernel will still be to all intents and
> purposes an ACK/GKI kernel (with the aim that Android/riscv64 devices
> will use GKI kernels), but since maintenance of an officially
> _labelled_ GKI kernel is more expensive, we're removing the sticker
> for now.

AI / ML

Alibaba Cloud

Xuantie C906 processor Tops MLPerf Tiny v0.7 Benchmark

codasip®

L31 and L11 RISC-V embedded cores enable AI/ML edge customization

Fraunhofer

RISC-V Processor Core of Fraunhofer IPMS now ready for Edge AI

ANDES TECHNOLOGY

AX45MPV RISC-V Multicore 1024-bit Vector Processor

SiFive

SiFive Intelligence X280 RISC-V processor picked for use in Google AI compute nodes

UNTETHER AI

Boqueria AI device features over 1400 RISC-V processors for at-memory compute

RISC-V

High Performance Computing

E4 Computer Engineering, with Università di Bologna and CINECA to build the first operational RISC-V based cluster targeted to the codesign of HPC applications

EPAC accelerators target HPC applications

Researchers from the Technical University of Munich (TUM) have designed a chip to implement post-quantum cryptography

Developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project

HPC-centric software test suite for GCC and LLVM

BCS-CNS and Intel plans to jointly set up a pioneering laboratory to develop a new generation of s RISC-V based supercomputers

Brazil?

RISC-V®


2023
RISC-V®


2024
RISC-V®

Premier Members

AKEANA

Alibaba Cloud

ANDES TECHNOLOGY
FOUNDING

BOSC
北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP

成为资本 CHENGWEI CAPITAL

Google
FOUNDING

HUAWEI

ICT
FOUNDING

Imagination

ISCAS

MINISTRY OF SCIENCE, TECHNOLOGY AND INNOVATION
BRAZILIAN GOVERNMENT
BRASIL
UNITING AND REBUILDING

intel

NVIDIA

Phytium 飞腾

Qualcomm
FOUNDING

RIOS

RISC-V®

bit.ly/soccer-chips-risc-v-and-brazil

Blog

Acura, part of HID, Collaborates with Von Braun Labs and #Data to Develop a RISC-V Based ASIC for Access Control and Free-Flow Tolling

September 28, 2023

By: Dario Sassi Thober, thober@vonbraunlabs.com.br & Rafael Vidal Aroca, aroca@vonbraunlabs.com.br

São Paulo, September 26th, 2023

Today's global landscape is saturated with access control systems. Acura, part of HID, is joining forces with von Braun Labs to engineer a novel semiconductor chip for this market segment. The project, rooted entirely in Brazil, will leverage the #Data ChipInventor EDA Platform and Manufacturing tools. The goal is to design a RISC-V compatible microprocessor, aiming to substantially decrease the costs associated with implementing concurrent technological platforms in Electronic Toll Collection and Access Control across varied applications.

The initial rollout for this solution will cater to Free-Flow / Open-Road Tolling initiatives, setting a global benchmark for Service Operators, Systems Integrators, and Infrastructure Companies in the Transportation and Mobility domains.

ChipInventor, a cloud-based semiconductor design tool, utilizes the unique #Data visual language. This enables chip design through a collaborative, block-based visual methodology. Beyond facilitating swift and efficient online semiconductor design – from rudimentary ASICs to comprehensive processors, like RISC-V microprocessors – ChipInventor also supports simulation, FPGA board prototyping, and final file synthesis for chip manufacturing. The platform is bundled with user-friendly compilers and toolchains for RISC-V device software development, making it an ideal choice for both professionals and newcomers. It's also well-suited for semiconductor training programs.

The RISC-V ISA provides a stable foundation for such products, its open standard nature showcasing its reliability for emerging embedded initiatives.

Escola Politécnica desenvolve chipset inovador para Internet das Coisas

Dispositivo coloca o Brasil na mesma página da tecnologia global, de acordo com o Ministério de Ciência, Tecnologia e Inovação

03/04/2024 - Publicado há 1 mês

Texto: Redação

Arte: Simone Gomes

In the News

BSC and Brazil's Instituto ELDORADO Collaborate to Advance RISC-V Development for HPC and AI

April 15, 2024

An international collaboration between BSC and Instituto ELDORADO will enable Brazil to develop open-source RISC-V technologies to accelerate research and development in the areas of semiconductors and supercomputing.

The primary goal of this project is to advance the fields of High Performance Computing (HPC) and artificial intelligence. It signifies the start of an initiative to develop a Matrix Multiplication Acceleration Unit that will be integrated into a RISC-V processor, pushing the boundaries of technology.

Read the full article.

DCC
DEPARTAMENTO DE CIÊNCIA DA COMPUTAÇÃO

DCC Cursos Pesquisa Parcerias

Laboratório de Compiladores do DCC/UFMG participa de projeto para criar microprocessador

RISC-V®

14 jun 2024
Instituto Eldorado

bit.ly/riscv-brasil

RISC-V®

Thanks!

Rafael Peria de Sene
Technical Program Manager
The Linux Foundation | RISC-V International
rsene@linuxfoundation.org or rafael@riscv.org
@rpsene
May, 2024